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㊹発明の名称　メモリ装置

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明　細　書

発明の名称

メモリ装置

特許請求の範囲

ロウ・アドレス・ストローブ・クロックとカラム・アドレス・ストローブ・クロックとを入力するマルチアドレス形式のメモリ装置において、前記二つのクロックを入力する第一のフリップフロップ回路と、書込イネーブル・クロックと出力イネーブル・クロックとの論理回路出力並びに前記第一のフリップフロップ回路出力の論理積を入力にし且つ複写モードとしてのデータ複写サイクル認識信号を出力する第二のフリップフロップ回路と、前記データ複写サイクル認識信号とロウ・アドレス、カラム・アドレス判定信号とをアドレスデコーダからの信号と比較するセレクタ回路とを有し、前記両クロックの立ち下がりエッジにおける他のクロックのレベルが特定の組合せになったとき、前記ロウ・アドレス・ストローブ・クロックおよび前記カラム・アドレス・ストローブ・クロックによりラッチされたアドレスをそれぞれ第一ロウ・アドレスおよび第二ロウ・アドレスとし、前記第一ロウ・アドレスによって指定された複数のメモリセル・データを前記第二ロウ・アドレスによって指定された複数のメモリセルにワード線単位で複写することを特徴とするメモリ装置。

発明の詳細な説明

〔産業上の利用分野〕

本発明はメモリ装置に関し、特に内部でデータの複写を行うメモリ装置に関する。

〔従来の技術〕

従来、メモリセルアレイ部を有するメモリ装置は、外部から与えられたデータを記憶し且つ記憶されたデータを外部へ読出す機能のみを有している。このメモリ記憶装置においては、データの記憶および読出にあたりロウ・アドレス・ストロー

ブ・クロックとカラム・アドレス・ストローブ・クロックとを入力するマルチアドレス形式を採用しているが、かかるメモリ装置において記憶されたデータを複写するときには、メモリ装置に接続された外部回路に一旦複写するためのデータを出力し、前記データの読出および書込機能を用いてデータを複写している。

〔発明が解決しようとする問題点〕

上述した従来のメモリ装置は、データを複写する際にデータがメモリ装置の外部回路を経由するため、一度に記憶したりあるいは一度に読出したりできるデータ量に対し記憶容量の大きなメモリ装置においては、もしくは記憶データの初期化を行うようにすべてのデータを書替えるような場合においては、データの複写を必要とする動作回数が多くなり、したがって複写時間全体が長くなるという欠点がある。

本発明の目的は、従来のかかる複写時間を短縮するメモリ装置を提供することにある。

〔問題点を解決するための手段〕

本発明のメモリ装置は、ロウ・アドレス・ストローブ・クロックとカラム・アドレス・ストローブ・クロックとを入力するマルチアドレス形式のメモリ装置において、前記二つのクロックを入力する第一のフリップフロップ回路と、書込イネーブル・クロックと出力イネーブル・クロックとの論理回路出力並びに前記第一のフリップフロップ回路出力の論理積を入力にし且つ複写モードとしてのデータ複写サイクル認識信号を出力する第二のフリップフロップ回路と、前記データ複写サイクル認識信号とロウ・アドレス，カラム・アドレス判定信号とをアドレスデコーダからの信号と比較するセレクタ回路とを有し、前記両クロックの立ち下がりエッジにおける他のクロックのレベルが特定の組合せになったとき、前記ロウ・アドレス・ストローブ・クロックおよび前記カラム・アドレス・ストローブ・クロックによりラッチされたアドレスをそれぞれ第一ロウ・アドレスおよび第二ロウ・アドレスとし、前記第一ロウ・アドレスによって指定された複数のメモリセル・データを前記第二ロウ・アドレスによって指定された複数のメモリセルにワード線単位で複写するように構成される。

〔実施例〕

次に、本発明の実施例について図面を参照して説明する。

第１図は本発明の一実施例を説明するための特定クロックのレベル判定論理回路図である。

第１図に示すように、かかるレベル判定論理回路は特定クロックとしての複写モードを表わすデータ複写サイクル認識信号を出力するための論理回路であり、ロウ・アドレス・ストローブ・クロック（以下、$\overline{\text{RAS}}$クロックと称す）の立ち下がりエッジにおいてカラム・アドレス・ストローブ・クロック（以下、$\overline{\text{CAS}}$クロックと称す）のレベルをラッチする第一のフリップフロップ１と、出力イネーブル・クロック（以下、$\overline{\text{OE}}$クロックと称す）および書込イネーブル・クロック（以下、$\overline{\text{WE}}$クロックと称す）の論理和の否定信号を出力する論理ＮＯＲゲート２と、第一のフリップフロップ１の出力とＮＯＲゲート２の出力との論理積をとる論理ＡＮＤゲート３と、$\overline{\text{CAS}}$クロックの立ち下がりエッジにおいてＡＮＤ３の出力をラッチする第二のフリップフロップ４と、$\overline{\text{RAS}}$クロックおよび$\overline{\text{CAS}}$クロックの論理和を出力する論理ＯＲゲート５とを有し、複写モード出力端子６にデータ複写サイクル認識信号を出力する。

次に、このレベル判定論理回路の動作について説明する。

この回路は$\overline{\text{RAS}}$クロックの立ち下がりエッジにおいて$\overline{\text{CAS}}$クロックが高レベルであり、且つ続く$\overline{\text{CAS}}$クロックの立ち下がりエッジにおいて$\overline{\text{OE}}$クロック，$\overline{\text{WE}}$クロックが共に低レベルの場合に複写モード信号であるデータ複写サイクル認識信号が高レベルになる。また、$\overline{\text{RAS}}$クロックおよび$\overline{\text{CAS}}$クロックが高レベルの場合に、複写モード信号であるデータ複写サイクル認識信号は低レベルになる。

次に、第２図は第１図に示すレベル判定論理回路の出力を用いるメモリセルアレイ部のアドレス

処理回路図である。

第２図に示すように、このアドレス処理回路はメモリセルアレイ部に対し、$\overline{CAS}$クロックによりラッチされたアドレスをカラムアドレスもしくは第二ロウアドレスとして処理する回路である。

第２図において、メモリセルアレイはワード線１２とビット線１３の交叉する各点にトランスファゲート１４とコンデンサ１５とからなる記憶素子が接続される。また、各ワード線１２にはワード線選択ゲート１６が接続され、一方各ビット線１３には、ここでは一本しか示していないが、ビット線選択ゲート１９が接続される。更に、アドレスデコーダ９はロウアドレスおよびカラムアドレス兼用のアドレスデコーダであり、ＮＯＲゲート１０からなるセレクタ回路１１はアドレスデコーダ９のアドレスデコード出力をワード線１２の選択ゲート１６あるいはビット線１３の選択ゲート１９へ切替て入力するためのセレクタである。また、センスアンプ１７は複数のビット線１３が接続され、ビット線１３上の電荷情報（電圧）を増幅するセンスアンプであり、遅延回路１８により$\overline{RAS}$クロックが供給される。

一方、ロウアドレス，カラムアドレス判定信号端子７に入力されるＲｏｗ／$\overline{Column}$信号は複写モード出力端子６に入力される信号との論理がＮＯＲゲート８によって決定されるが、このＲｏｗ／$\overline{Column}$信号はアドレスデコーダ９へのアドレス入力が$\overline{RAS}$クロックの立ち下がりエッジでラッチされたものである（Ｒｏｗ）か、あるいは$\overline{CAS}$クロックの立ち下がりエッジによりラッチされたものである（Ｃｏｌｕｍｎ）かを示す信号である。

要するに、本実施例においては、第１図に示す複写モード信号によりＲｏｗ／$\overline{Column}$信号を制御する論理ＮＯＲゲート８を設け、これによりセレクタ回路１１のＮＯＲ１０にアドレスデコーダ９からのアドレスデコーダ信号との選択を行わせるようにしている。尚、上述したメモリ装置の回路動作については、次の第３図を参照して説明する。

第３図は第１図および第２図に示した回路におけるデータ複写時の主要信号波形図である。

第３図に示すように、$\overline{RAS}$クロックの立ち下がりエッジ（時刻t_1）において第一ロウアドレスがラッチされ、この第一ロウアドレス２０に対応したワード線（ＷＬ１）が適当な時刻において高レベルになる。しかる後、メモリセルを構成するトランスファゲート１４の電荷情報がビット線１３に達した時刻にセンスイネーブル信号（$\overline{SEN}$）を低レベルにし、ビット線の電荷情報（電圧）を増幅する。一方、時刻t_1における$\overline{CAS}$クロックが高レベルで且つ$\overline{CAS}$クロックの立ち下がりエッジ（時刻t_2）における$\overline{OE}$クロックおよび$\overline{WE}$クロックが共に低レベルであれば、時刻t_2の第二のロウアドレス２１をラッチする。従って、メモリ装置の内部では複写モード信号が高レベルになり、データを複写する特定のサイクルであることを認識することができる。しかるに、第２図に示すセンスアンプ１７が一度増幅動作を始めると$\overline{RAS}$クロックが高レベルになるまで増幅されたデータは失われないため、時刻t_2以後の適当な時刻において第二のロウアドレス２１に対応したワード線ＷＬ２が高レベルになると、蓄積されていた電荷情報が失われ、センスアンプ１７が増幅した電荷情報、すなわち第一ロウアドレス２０のメモリセルに蓄積されていた電荷情報に置き替わる。最後に、$\overline{RAS}$クロックの立ち上がりエッジ（時刻t_3）以後適当な時刻において、第一ロウアドレス２０に対応したワード線ＷＬ１および第二のロウアドレス２１に対応したワード線ＷＬ２が共に低レベルになり、且つセンスイネーブル信号（$\overline{SEN}$）が高レベルになることにより、この新たに設定した複写サイクルが終了する。

上述したように、本実施例においては、従来のメモリ装置では使用されていなかった$\overline{CAS}$クロックの立ち下がりエッジで$\overline{OE}$クロックおよび$\overline{WE}$クロック共に低レベルであるという特定クロックタイミングを複写サイクルの規定に用いているため、この新しいサイクルがメモリ装置の動作を

損うこともない。

〔発明の効果〕

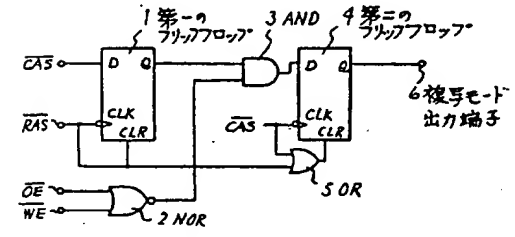
以上説明したように、本発明のメモリ装置は二つのフリップフロップ回路とセレクタ回路およびロウ・アドレス・ストローブ・クロック，カラム・アドレス・ストローブ・クロックを用い、前記両クロックの立ち下がりエッジにおける他のクロックのレベルが特定の組合せになったときにカラム・アドレス・ストローブ・クロックの立ち下がりエッジで第二ロウ・アドレスをラッチし、ロウ・アドレスに対応したワード線の単位でデータを内部複写することにより、一度に大量のデータを複写することができるようになるので、複写時間を短縮することができるという効果がある。

図面の簡単な説明

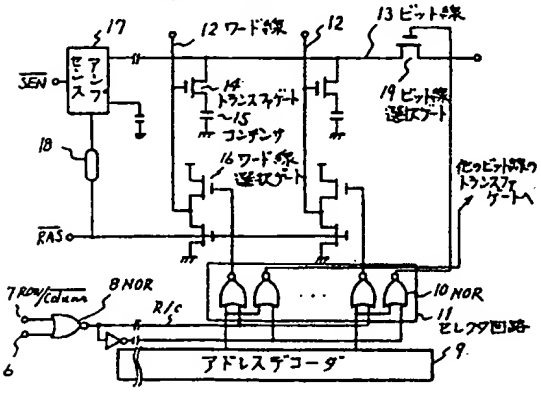
第１図は本発明の一実施例を説明するための特定クロックのレベル判定論理回路図、第２図は第１図に示すレベル判定論理回路の出力を用いるメモリセルアレイ部のアドレス処理回路図、第３図は第１図および第２図に示した回路におけるデータ複写時の主要信号波形図である。

1･･･第一のフリップフロップ、2･･･ＮＯＲ、3･･･ＡＮＤ、4･･･第二のフリップフロップ、5･･･ＯＲ、6･･･複写モード出力端子、7･･･ロウアドレス，カラムアドレス判定信号端子、8･･･ＮＯＲ、9･･･アドレスデコーダ、10･･･ＮＯＲ、11･･･セレクタ回路、12･･･ワード線、13･･･ビット線、14･･･トランスファゲート、15･･･コンデンサ、16･･･ワード線選択ゲート、17･･･センスアンプ、18･･･遅延回路、19･･･ビット線選択ゲート、20･･･第一のＲｏｗアドレス、21･･･第二のＲｏｗアドレス。

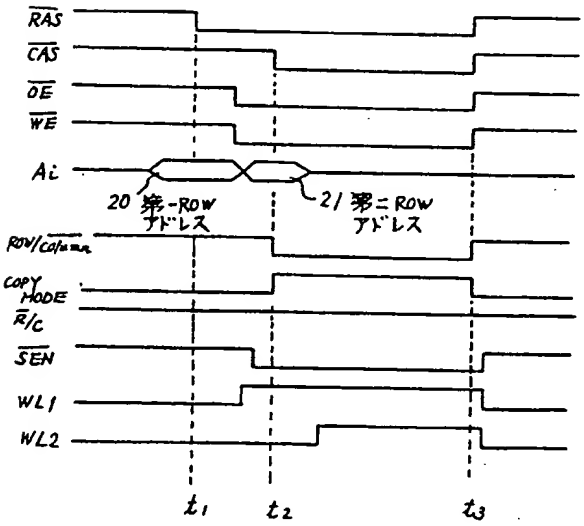
代理人　弁理士　内　原　　晋



第１図



第２図



第３図

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(54) Title of the Invention: MEMORY DEVICE

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Specification

Title of the Invention

Memory device.

Scope of the Patent Claims

A memory device characterized as a multi-address type memory device that inputs both row address strobe clock and column address strobe clock, and having a first flip-flop circuit into which the two aforementioned clocks are input, a second flip-flop circuit having as input the logical product of the logic circuit output of the write-in enable clock and of the output enable clock, as well as the output of the aforementioned first flip-flop circuit; moreover, a data copy cycle acknowledgement signal is output as a copy mode, and a selector circuit that compares the aforementioned data copy cycle acknowledgement signal and the row address column address deciding signal to a signal from the address decoder, and when the level of another clock is specifically combined to the trailing edges of both aforementioned clocks, the addresses latched by the aforementioned row address strobe column clock and the aforementioned column address strobe clock become, respectively, a first row address and a second row address, and the multiple memory cell data designated by the aforementioned first row address is copied in word line units into the multiple memory cells designated by the aforementioned second row address.

(Industrial Sector Where Used)

The present invention concerns a memory device, and in particular a memory device inside of which data is copied.

(Prior Art)

Conventional memory devices with a memory cell array only have a function whereby data provided from outside is recorded, and recorded data is read-out to the outside. For data recording and readout, such memory devices use a multi-address format to input row address strobe clock and column address strobe clock. In terms of copying data with these memory devices, though, data for one-time copying is output to an external circuit connected to the memory device, and the data is copied using functions to read-out and write-in the aforementioned data.

(Problems the Invention Endeavors to Resolve)

With the conventional type of memory device discussed above, data travels by way of the memory device's external circuit when data is copied. Thus, in a memory device having a large capacity memory to cope with a data volume capable of handling one-time recordings and one-time readouts, or for cases when all data is rewritten so as to initialize recorded data, copying data requires a large number of repeated operations, the drawback being that the overall copy time becomes lengthy.

The aim of the present invention is to provide a memory device that reduces copying time.

(Means to Resolve Problems)

The structure of the memory device of the present invention comprises a multi-address format memory device that inputs row address strobe clock and column address strobe clock and that has a first flip-flop circuit into which are input the two aforementioned clocks, a second flip-flop circuit having as input the logical product of the logical circuit output of the write-in enable clock and of the output enable clock, as well as the output of the aforementioned first flip-flop circuit and, as a copy mode, a second flip-flop circuit that outputs a data copy cycle acknowledgment signal, and a selector signal that compares the aforementioned data copy acknowledgement signal and the row address column address deciding signal to a signal from the address decoder, and when another clock level is specifically combined at the trailing edges of the two aforementioned clocks, addresses latched by the aforementioned row address strobe clock and the aforementioned column address strobe clock are deemed as, respectively, a first row address and a second row address, and the multiple memory cell data designated by the aforementioned first row address can then be copied as word line units into the multiple memory cells designated by the aforementioned second row address.

(Embodiments)

Next, the present invention will be explained while referring to figures.

Figure 1 is a level-deciding logic circuit diagram for a specific clock to explain one embodiment of the present invention.

As shown in Figure 1, this sort of level-deciding logic circuit is a logic circuit to output a data copy cycle acknowledgement signal to express the copy mode of a specific clock, and has a first flip-flop (1) to latch the level of the column address strobe clock (hereafter referred to $\overline{CAS}$ clock) to the trailing edge of the row address strobe clock (hereafter referred to as $\overline{RAS}$ clock), a logic NOR gate (2) to output the negation signal of the logical sum of the output enable clock (hereafter referred to as $\overline{OE}$ clock) and the write-in enable clock (hereafter referred to as $\overline{WE}$ clock), a logic AND gate (3) that derives the logical product of the output of the first flip-flop (1) and of the output of the NOR gate (2), a second flip-flop (4) that latches the output of AND gate (3) to the trailing edge of the $\overline{CAS}$ clock, and a logic OR gate (5) to output the logical sum of the $\overline{RAS}$ clock and the $\overline{CAS}$ clock, whereby a data copy cycle acknowledgement signal is output to the copy mode output terminal (6).

Following is an explanation of how this level-deciding logic circuit operates.

This circuit is such that $\overline{CAS}$ clock is high-level at the trailing edge of $\overline{RAS}$ clock. Moreover, when $\overline{OE}$ clock and $\overline{WE}$ clock are both low-level at succeeding $\overline{CAS}$ clock trailing edges, the data copy cycle acknowledgement signal that serves as a copy mode signal becomes high-level. Further, when $\overline{RAS}$ clock and $\overline{CAS}$ clock are high-level, the data copy cycle acknowledgement signal that serves as the copy mode signal becomes low-level.

Figure 2 is an address processing circuit diagram of a memory cell array component that uses the output of the level-deciding logic circuit depicted in Figure 1.

As shown in Figure 2, this address processing circuit is a circuit whereby an address latched by $\overline{CAS}$ clock to the memory cell array is processed as a column address or a second row address.

In Figure 2, storage cells comprising transfer gates (14) and condensers (15) are connected to the different points at which word lines (12) and bit lines (13) intersect. Also, word line selection gates (16) are connected to the various word lines (12), while bit line selection gates (19) (though only one is shown here) are connected to the various bit lines. Furthermore, address decoder (9) is an address decoder that jointly uses a row address and a column address, and the selector circuit (11) comprising NOR gate (10) is a selector whereby the address decoder output of address decoder (9)

is switched to the selection gates (16) of the word lines (12) or to the selection gates (19) of the bit lines (13). Also, the sense amp (17) is one whereby multiple bit lines (13) are connected, the charge information (voltage) on the bit lines (13) is amplified, and $\overline{RAS}$ clock is supplied by a delay circuit (18).

The logic of the Row/Column signal input to the row address/column address determination signal terminal (7) with the signal input to the copy mode output terminal (6) is determined by the NOR gate (8). This Row/Column signal is a signal that indicates whether address input to the address decoder (9) is latched to the trailing edge of the $\overline{RAS}$ clock (Row) or to the trailing edge of the $\overline{CAS}$ clock (Column).

In short, a logic NOR gate (8) that controls the Row/Column signal by means of a copy mode signal shown in Figure 1 is provided in the present embodiment, whereby the NOR (10) selector circuit (11) selects the address decoder signal from the address decoder (9). The circuit operations of the memory device discussed above will now be explained referring to Figure 3.

Figure 3 is a waveform diagram of the main signals at data copy time in the circuits shown in Figure 1 and in Figure 2.

As shown in Figure 3, a first row address is latched at the trailing edge (time t_1) of the $\overline{RAS}$ clock, and the word line (WL1) that corresponds to this first row address (20) becomes high-level at the proper time. Thereafter, when the charge information of the transfer gate (14) comprising the memory cell reaches the bit lines (13), the sense enable signal ($\overline{SEN}$) becomes low-level and the charge information on the bit line (voltage) is amplified. Moreover, if $\overline{CAS}$ clock at time t_1 is high-level and both the $\overline{OE}$ clock and the $\overline{WE}$ clock are low-level at the trailing edge (time t_2) of the $\overline{CAS}$ clock, the second row address (21) of time t_2 is latched. Inside the memory device, then, the copy mode signal becomes high-level, and acknowledgement as to whether it is a specific copy data cycle can occur. However, once the sense amp (17) shown in Figure 2 starts amplification operations, amplified data is lost until $\overline{RAS}$ clock reaches high-level. Thus, when the word line (WL2) corresponding to the second row address (21) reaches high-level at the proper time after time t_2, the accumulated charge information is lost and rewritten into the charge information amplified by the sense amp (17), namely the charge information accumulated in the memory cells of the first row

address (20). Thereafter, at a proper time (time t_3) following the trailing edge of the $\overline{RAS}$ clock, the word line (WL1) corresponding to the first row address (20) and word line (WL2) corresponding to the second row address both become low-level. Moreover, this newly set copy cycle ends after the sense enable signals ($\overline{SEN}$) become high-level.

The present embodiment involves a specific clock timing not used in conventional memory devices whereby both $\overline{OE}$ clock and $\overline{WE}$ clock are low-level at the trailing edges of $\overline{CAS}$ clock. This timing is used to regulate copy cycles. Thus, there are no operational failures in the new cycle.

(Outcomes of the Invention)

As explained above, the memory device of the present invention uses two flip-flop circuits and a selector circuit, as well as row address strobe clock and column address strobe clock, and when another clock level is specifically combined with the trailing edges of the two aforementioned clocks, the second row address is latched to the trailing edge of the column address strobe clock and, by internally copying data as word line units corresponding to the low address, a large volume of data can be copied at once, the outcome thus being reduced copying time.

Brief Description of the Figures

Figure 1 is a level-deciding logic circuit diagram for a specific clock. Figure 2 is an address processing circuit diagram of the memory cell array part using the output of the level deciding logic circuit shown in Figure 1. Figure 3 is a waveform diagram of the main signals during data copying in the circuits shown in Figure 1 and Figure 2.

(1) ... first flip-flop; (2) ... NOR; (3) ... AND; (4) ... second flip-flop; (5) ... OR; (6) ... copy mode output terminal; (7) ... row address/column address deciding signal terminal; (8) ... NOR; (9) ... address decoder; (10) ... NOR; (11) ... selector circuit; (12) ... word line; (13) ... bit line; (14) ... transfer gate; (15) ... condenser; (16) word line selection gate; (17) ... sense amp; (18) ... delay circuit; (19) ... bit line selection gate; (20) ... first row address; (21) ... second row address.

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[0005]

Data are deleted when high electric potential is applied to a p-type substrate (n-type substrate and a p-type well in the case of well structure) and the control gates of all the memory transistors as well as the gates of selection gate transistors are made to be 0V. As a result, electrons in the floating gates are discharged to the substrate in all the memory transistors and the threshold value moves in the negative direction.

[0006]

Data are read when non-selection memory transistors which are closer to the bit line than selection gate transistors and the selection memory transistors are made to be "on" and 0V is applied to the gates of the selection memory transistors. In this case, discrimination of "0" or "1" is accomplished by reading the electric current running flowing through the bit line.

[0007]

As explained above, in an NAND cell-type EEPROM, intermediate electric potential must be applied to a bit line for which writing is not executed during the data writing mode. For this reason, the structure of a peripheral circuit of memory cell array becomes complicated. Moreover, the timing of applying intermediate electric potential becomes difficult to control. In fact, unless the intermediate electric potential to be applied to the bit line is not raised before the control voltage to be applied to the control gate line, a writing error may occur. Moreover, in order to apply intermediate electric potential properly, it becomes necessary to prevent punch-through of the selection gate transistors. Hence, the gate length of the selection gate transistors cannot be made too short. This becomes an obstacle for achieving EEPROM with very high density.

[0008]

Above problems are not limited to NAND cell-type EEPROM, but occur also in NOR-type EEPROM in which memory cells are made of one memory transistor and one selection gate transistor based on a similar principle.

[0009]

[Problems Overcome by the Invention]

As explained above, in the EEPROM of the prior art, it was necessary to apply intermediate electric potential to the bit line during data writing, which resulted in complicated peripheral circuits and difficult timing control. Hence, the gate length of selection gate transistors could not be made shorter, which was a serious problem. The present invention aims to provide an EEPROM in which the above problems are resolved.

[Construction of the Invention]

[0010]

[Problem Resolution Means]

In the present invention, EEPROM is structured with a memory cell array wherein at least one memory transistor with an electric charge storage layer and a control gate and a memory cell made of a selection gate transistor which is connected in series with the memory transistor are arranged in a matrix, with the drains of the selection gate transistors lined up in the row-direction of the memory array being jointly connected to the bit line, and with the gate of the memory transistors which are lined up in the column-direction of the memory cell array and the gate of the selection gate line being jointly connected to the control gate line and the selection gate line respectively, and a bit line electric potential control means is provided for setting the bit line to the low electric potential state or a floating state depending upon the data during the data writing time.

[0011]

[Operation]

In the EEPROM of the present invention, the bit line (the bit write for "1" data writing) connected to the memory transistors which execute electric potential injection during data writing is made to be 0V, while the bit line (the bit line for "0" data writing) connected to the memory transistor which does not execute electron injection is made

to be the floating state. Such electric potential control of the bit line may be enabled by providing, for example, a bit line selection gate transistor between the edge section of the bit line and the bit line driving circuit to be connected to the bit line. In this case, both the drain and source dispersion layers are also in the floating state in the memory transistors along the bit line which is in the floating state, and the electric potential of the drain and the source layers also rise because the high electric potential of the control gate line is capacity coupled. Hence, electron injection to the floating gate is prevented.

[0012]

Hence, in the EEPROM of the present invention, instead of applying intermediate electric potential to the bit line to be connected to memory transistors for which tunnel injection is desired not to occur, the bit line is made to be floating. As a result, the peripheral circuit becomes simple and it becomes unnecessary to make the gate length of the selection gate transistors longer to prevent punch-through.

[0013]

[Embodiment]

An embodiment of a NAND cell-type EEPROM having n-channel FETMOS as memory transistors is described hereafter, with reference to the drawings.

[0014]

Fig. 1 is an equivalent circuit of describing major structure of NAND cell-type EEPROM in an embodiment of the present invention, Fig. 2 is a flat view of one NAND cell section, and Fig. 3 and Fig. 4 are respective cross sections of Fig. 2 relative to lines A-A' and B-B'.

[0015]

Fig. 1 shows that the memory array 21 is composed of a matrix arrangement of NAND cells. In this embodiment, the NAND cell comprises four memory transistors M1. M2. M3 and M4 which are connected in series, and selection gate transistors Qs1 and Qs2

which are provided on both sides of the memory transistors. The drain sides of the NAND cells which are lined up in the row-direction of the memory cell array 1 are jointly connected to the bit line BL through the selection gate transistor Qs1. The control gate lines CG1, CG2, CG3 and CG4, and the selection gate lines SG1 and SG2 are provided in such a manner that the control gate of each memory transistor and the gate of the selection gate transistor are jointly connected to each NAND cell which is lined up in the column-direction of the memory cell array 1.

[0016]

The bit line BL (BL1, BL2, ..., BLm) are respectively connected to the bit line driving circuit 22 (221, 222, ...22m) at one edge section of the memory cell array 1. In the present invention, bit line selection transistors QBL (QBL1, QBL2, ..., QBLm) are provided between the bit line driving circuit 22 and the bit line BL.

[0017]

The structure of an NAND cell is explained hereafter, with reference to Fig. 2 ~ Fig. 4. On n-type silicon substrate 1, p-type well 2 is formed, and four memory transistors M1 ~ M4 and two selection gate transistors Qs1 and Qs2 are provided in a region divided by an element isolation insulating film 13. In each memory transistor floating gates 4 (41 ~ 44) with first layer polycrystal silicon are formed through thin gate insulation film 31 which is formed on the substrate by heat oxidation, and control gates 6 (61 ~ 64) with a second layer polycrystal silicon are laminated in-between insulating film 5 on top of the floating gate 4. The floating gate 4 is the electric charge storage layer.

[[0018]

The control gates 6 of each memory transistor are provided as continuous control gate line CG (CG1 ~ CG4) for NAND cell which are arranged in horizontal direction. In general, these control gate lines CG are the word lines.

[0019]

The n-type layer 8, which are the source and drain dispersion layers of the memory transistor, are shared by adjacent ones and four transistor memories M1 ~ M4 are

connected in series. For drain side and source side of these four memory transistors, respective selection gate transistors Qs1 and Qs2 are provided. The gate insulation film 32 of these selection gate transistors Qs1 and Qs2 are formed to be thick, independent of the memory transistor M, and two layers of gate electrodes 45,65 and 46, 66 are formed on top of the gate insulation film 32. These gate electrodes 45, 65 and 46, 66 are formed by simultaneously patterning the first layer polycrystal silicon and the second layer polycrystal silicon which comprise the floating gate and the control gate of the memory transistor. These two-layer gate electrodes are continuously arranged in the direction of the control gate CG while contacting each other at predetermined intervals, and become the selection gate lines SG1 and SG2.

[0020]

The top of the device-formed substrate is covered with CVD insulation film 11 and the bit line 12 is provided by means of Al film and the like on top of the CVD film. The bit line 12 makes contact with the drain dispersion layer 9 of the selection gate transistor Qs1. In order to strengthen contact, n-type impurity is repeatedly doped onto the drain dispersion layer 9 through the contact hole. The source dispersion layer 10 of the other selection gate transistor Qs2 is normally jointly provided in a plurality of NAND cells as common source lines.

[0021]

The coupling capacity between the floating gate 4 and the control gate in each memory transistor is set to be larger than that between the floating gate 4 and the p-type well 2 by extending the arrangement of the floating gate 4 in the element-isolated region. As for the actual dimensions; the width of the floating gate 4 and the control gate 6 is 1μs respectively, hence the channel length of the memory transistor is 1μs and one side of each floating gates 4 is extended by 1μs on the element-isolated region film 13. The gate insulation film 31 under the floating gate 4, for example, is heat oxidation film of 10nm and the in-between layer insulation film 5 is heat oxidation of 25nm.

[0022] The operation of the NAND cell-type EEPROM in the embodiment is described hereafter with reference to Fig. 5 with focus on the NAND cell composed of the memory transistors M1 ~ M4. Fig. 5 is a timing drawing illustrating a series of operations-- data deletion, data writing and data reading. Data deletion and data writing are executed through electric charge exchange using F-N tunneling between the floating

gate and the p-type well in the memory transistor.

[0023]

Initially, the data deletion is executed by making all the control gate lines CG1 ~ CG4 0V, and by applying high electric potential of Vwell = Vsub = 18V to the p-type well 2 and p-type silicon substrate 1. At this time, high electric potential of 18V is also simultaneously applied to the selection gate lines SG1 and SG2. As a result, electrons of the floating gates are discharged to the p-type cell in all the memory transistors that comprise the memory cell, and deletion state ("0") in which the threshold value is moved in negative direction is achieved.

[0024]

Data writing is executed starting with the bit line which is farthest away from the memory transistor. First, for the writing at the memory transistor M4, high electric potential of 20V is applied to the selection gate line CG4, intermediate electric potential of 10V are applied to all other control gate lines CG1 ~ CG3 and the selection gate line SG1, and the bit line is set to be 0V (in the case of "1") or floating (in the case of "0"). At this time the bit line electric potential is executed by on-off control of the bit line selection transistor QBL. Fig. 5 describes the condition in which the electric potential VSG11 of the selection gate line SG11 in the bit line selection transistor QBL1 is set to be 5V and 0V, which is an output electric potential corresponding to the data "1" of the bit line driving circuit 221, is transmitted to the bit line BL1, and the condition in which the electric potential VSG12 of the selection gate line SG12 in the adjacent bit line selection transistor QBL2 is set to be 0V and the bit line BL2, being isolated from the bit line driving circuit 221, becomes floating state.

[0025]

As a result, in the memory transistor M4, where 0V is applied to the bit line, electrons are tunnel injected from the drain to the floating gate and the condition ("1") in which threshold value moves to the positive direction is obtained. When the bit line is in the floating state, the electric potential of the drain and source dispersion layers rises due to capacity coupling with the control gate, hence, tunnel injection does not occur and the threshold value does not change. Subsequently, high electric potential is provided to the control gates CG3, CG2 and CG1 and data writing is executed in a similar

manner.

[0026]

Data reading is executed by applying 0V to selected control gate line, which in turn provides an electric potential of about 5V in the control gate line on the bit line side and an electric potential of about 1 – 5 V to the bit line, and by detecting whether or not the electric current is flowing through the bit line.

[0027]

As explained above, in the present embodiment, instead of providing intermediate electric potential to the bit line in which writing is not desired during data writing, the bit line is set to be floating. As a result, an electric potential of 5V, electric potential during data reading, or higher is not applied to the bit line. Hence, it becomes unnecessary to use intermediate electric potential and the peripheral circuit becomes simpler. Moreover, it is not needed to set punch-through prevention pressure unnecessarily high in the selection gate transistor on the bit line side, allowing the length of the gate to be the same as the length of the selection gate transistor on the source side. As a result, an EEPROM with very high density is achieved.

[0028]

The application of the present invention is not limited to aforementioned embodiment. In fact, in the present embodiment the bit line selection gate transistor is provided in the vicinity of the memory cell array, but the bit line selection gate transistors may be arranged for each block if the memory cell is divided into blocks. Moreover, instead of providing bit line selection gate transistors as means to control the bit line electric potential including making the bit line floating

state, the bit line driving circuit itself may be provided with an ability to change the output terminal into floating state.

[0029]

Furthermore, in the present embodiment, only NAND cell-type EEPROM is described,

but the present invention may similarly be applied to a NOR-type EEPROM in which the memory cell consists of one memory transistor and one selection gate transistor.

[0030]

[Efficacy]

As explained above, the present invention simplifies peripheral circuits by providing bit line electric potential control means that changes the bit line on which data are desired not to be written during data writing into floating state, which leads to achievement of EEPROM with very high density.

[Brief Description of Drawing]

[Fig. 1] An equivalent circuit drawing of NAND cell-type EEPROM of an embodiment of the present invention.

[Fig. 2] A flat view illustrating a structure of NAND cell in the embodiment.

[Fig. 3] A cross-section of Fig. 2 relative to A-A'.

[Fig. 4] A cross-section of Fig. 2 relative to B-B'

[Fig. 5] A timing chart illustrating operation of EEPROM in the embodiment.

[Explanation of Symbols]

1. n-type silicon substrate
21. Memory cell array
2. p-type well
22. Bit line driving circuit
3. Gate insulation film.
BL. Bit line
4. Floating gate
CG. Control gate line
5. In-between layer insulation film
SG. Selection gate line
6. Control gate
QBL. Bit line selection transistor
8~10 n-type dispersion layer
11. CVD insulation film
12. Bit line
13. Element-isolation insulation film